ESD Sensitivity of Precision Chip Resistors Comparison between Foil and Thin Film Chips

By Joseph Szwarc, 2008

ABSTRACT

The sensitivity level of resistors used in electronic equipment to an electrostatic discharge (ESD) varies from a few hundred volts to a few tens of kilovolts. Ways to make resistors more robust to ESD are suggested. The influence on ESD robustness of resistive element's size, resistive pattern design and ohmic value is discussed. Foil and Thin Film technologies are compared.

In order to test the capability of high precision resistor chips to withstand high voltage ESD, samples were chosen from Bulk Metal Foil® technology and two types of Thin Film material - nickel-chrome alloy and Tantalum nitride. identically sized chips of two ohmic values - 30 Ω and 1 kΩ - were tested.

All samples underwent ESD pulses ranging from 2 kV to 24 kV. Test results indicated two orders of magnitude superior stability of Foil chips over Thin Film chips when subjected to high voltage ESD, for both ohmic values. This superiority is attributed mainly to lower temperature rise due to the much larger thickness and therefore heat capacity of the resistive Foil layer compared to Thin Films.

INTRODUCTION

The most common mode of failure of electronic devices due to ESD is the rupture or evaporation of a thin dielectric or oxide layer of a semiconductor by the high voltage spike. Resistors used in electronic devices are more robust than semiconductor devices, but are still not exempt from failure caused by ESD. Their main failure mode is fusing of the resistive material at a weak point of the resistive pattern - the “hot spot” - due to the high temperature rise resulting from high energy density and the near-adiabatic characteristic of the process.

Manufacturers test for ESD sensitivity (ESDS) per customer request, but usually do not publish ESDS specifications in their data sheets. Standards dealing with resistors have only recently started defining specifications linking ESD test voltage levels to the size of resistor chips.

The ESDS of precision chip resistors depends on the production technology, on the chip’s size, on the resistor’s ohmic value, on the resistive layer’s thickness, and on the design of the resistive pattern. In testing the influence of above factors, the results depend also on the test method used. A 1989 IEEE paper (see ref. #1) deals with ESDS of passive Thin Film components, among them Tantalum nitride hybrid chip resistors. An update is made here, to account for the developments in the fields of:

- Technologies of electronic component assembly methods
- Technologies of production of precision chip resistors
- Standards concerning ESD susceptibility of resistors and ESD test methods

TECHNOLOGIES OF COMPONENT ASSEMBLY METHODS

The most popular electronic assembly method today is the surface mount technology, SMT. Manufacturers of components responded to this trend by developing standard sizes of surface mounted chips. Miniaturization leads to the use of smaller sized SMT chips and this causes an increase in the sensitivity of electronic equipment to ESD.

ESD voltage levels which do not affect larger resistor chips may be dangerous for smaller sizes because of their smaller heat capacity.

PRODUCTION TECHNOLOGIES OF PRECISION CHIP RESISTORS AND THEIR INFLUENCE ON ESD SENSITIVITY

The table below shows typical specifications for two main technologies used in production of precision surface mounted chip resistors: Bulk Metal Foil and Thin Film.

TABLE 1 - ELECTRICAL SPECIFICATIONS OF FOIL AND THIN FILM CHIPS

PRODUCT TECHNOLOGY	BEST TCR, MIL. RANGE	RANGE OF OHMIC VALUES, ALL CHIP SIZES
Bulk Metal Foil	0.2 ppm/°C	5 Ω to 150 kΩ
Thin Film	10 ppm/°C	30 Ω to 3 MΩ

Foil chips are produced by cementing a nickel-chromium alloy foil, rolled to a thickness between 2 and 10 microns, to a ceramic substrate. Thin Film chip production involves deposition (by evaporation, sputtering or similar methods) on a ceramic substrate of a film, mainly nickel-chromium or Tantalum Nitride. A typical thickness of the Thin Film layer is about 1/100 of the 2.5 microns thick foil.

ESD Sensitivity of Precision Chip Resistors
Comparison between Foil and Thin Film Chips

TABLE 2 - CHIP RESISTOR STYLES, ASSIGNED ESD TEST VOLTAGE AND ENERGY DENSITY

STYLE		RESISTIVE LAYER'S DIMENSIONS (1) (mm)	LAYER'S AREA (mm^2)	ESD TEST VOLTAGE (2) (V)	ESD ENERGY (E mJ)	ENERGY DENSITY (E mJ/mm^2)
METRIC	INCHES					
RR1005M	RR0402	0.5 x 0.5	0.25	500	0.019	0.076
RR1608M	RR0603	1 x 0.8	0.8	1000	0.075	0.094
RR2012M	RR0805	1.4 x 1.2	1.7	1500	0.169	0.100
RR3216M	RR1206	2 x 1.6	3.2	2000	0.300	0.094
RR5025M	RR2010	4 x 2.5	10	3000	0.675	0.068

Notes

(1) Approximate dimensions of the part of chip's surface occupied by the pattern, in mm

(2) Per draft International Standard prEN140401-801:200X

Chips are made in standardized sizes (see table 2 and ref. #2), in rectangular shapes. In the middle of the rectangle is a pattern formed in the resistive layer of Foil or Thin Film, connected on two sides to two termination pads. In case of a blank rectangle pattern, the chip's resistance value is estimated by dividing this rectangle's length by its width to obtain the "number of squares". The resistance of such a square in ohms per square is called sheet resistance and can be equal, depending on layer's thickness, to between 0.1 and 0.6 for Foil or 40 and 300 for Thin Film.

In order to achieve higher resistance values, a meandering pattern of lines and end loops is formed in the resistive layer (see fig. 1 and 2). Values of resistance achieved will increase proportionally to the length of the path divided by its width - or number of squares.

Fig. 1 shows a high ohmic value Thin Film pattern with an initial 500 squares of resistance. As the lines and the spaces between pattern's lines are of similar width, the lines occupy less than half of the area between the two pads. On the right side of the pattern, one shunting loop (out of 17) has been cut, adding about 130 squares. Next right is the "ladder" with 12 rungs cut, each adding about 10 squares. Next a bar called a "top hat" has a laser cut kerf adding about 6 squares and finally the cut into the last, wide bar brings the resistance to its target value.

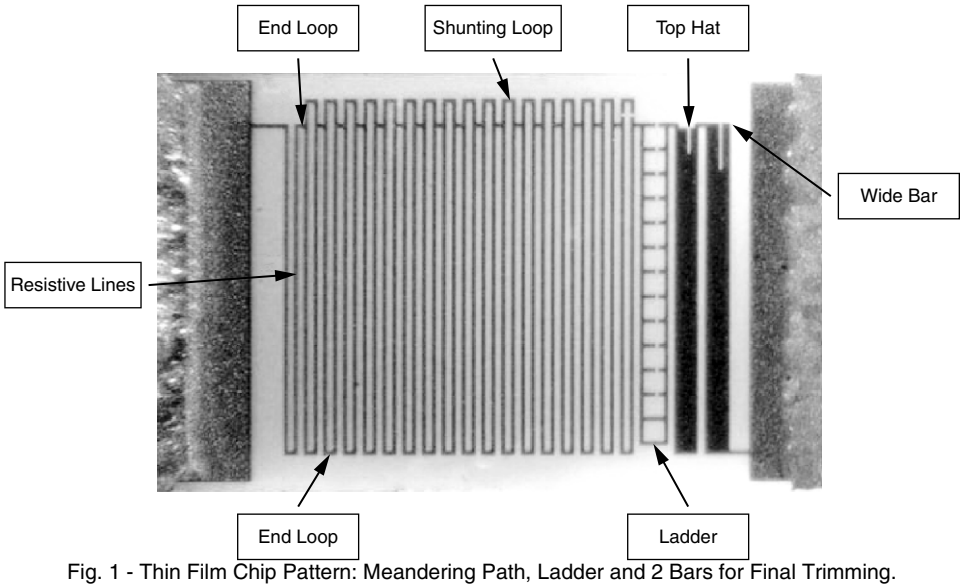

Fig. 1 - Thin Film Chip Pattern: Meandering Path, Ladder and 2 Bars for Final Trimming.

Thin Film pattern per fig. 2 is used for low ohmic values. Compared to fig. 1, a larger area is covered by the resistive pattern because the kerfs occupy only a small part of the area.

ESD Sensitivity of Precision Chip Resistors Comparison between Foil and Thin Film Chips

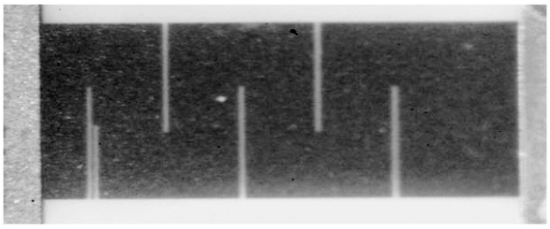

Fig. 2 - Blank Image, Laser Trimmed. Final Trim Performed by a Second Cut in the Left Kerf.
It can provide between 1.66 and 20 Squares of Resistance.

As the Foil is 100 times thicker than Thin Film, a given pattern in Thin Film will produce a resistance value 100 times higher than in Foil. To achieve the same value of resistance, the Foil's meandering pattern will need to consist of much larger number of narrower lines than the Thin Film's pattern.

The Thin Film resistive pattern for high ohmic values (see fig. 1) is designed with all or a part of pairs of lines short-circuited by shunting loops so as to allow, by cutting these loops (an operation called trimming, usually by laser), to reach the desired target resistance value. The shorted lines do not participate in dissipation of heat and as a result the ESD energy is confined to the shunting loops and a few lines only - a small part of the pattern's area - causing an increase in energy density. In a pattern designed to cover a wide range of target resistance values (by shorting all adjacent end loops), but trimmed to a value close to the low end of the range, only a small part of the pattern will be active and will absorb the total ESD energy, thus increasing the energy density and the temperature rise. Foil patterns are designed with a narrow range of values, allowing for a better utilization of the total area and reducing the energy density.

Additional temperature rise occurs in the "hot spots" - points of high current density. This is due to current crowding where the current changes direction and where a line is narrowed or layer's thickness is reduced due to a production defect. Proper design can reduce this crowding. Detailed description of resistor technologies can be found in ref. 3.

CALCULATION OF TEMPERATURE RISE IN THE RESISTIVE MATERIAL

Based on the energy density estimate in table 2 and the above considerations of energy distribution on the chip's surface it is possible to estimate the theoretical ESD induced adiabatic temperature rise in the resistive foil. Actual temperature rise will be lower, because low values suffer short pulses but only a part of the energy, while high values absorb the full energy of discharge, but longer pulses (see below). For ease of calculation units used will be:

- cm^3 for foil's volume, v
- J/cm^2 for energy surface density, e
- $J/(cm^3 \times °C)$ for foil's volumetric specific heat, c_{fv}

For our calculation we choose from table 2 the largest value of the energy density: $e = 0.1\ mJ/mm^2 = 0.01\ J/cm^2$

Specific heat of the Ni/Cr alloy $c_{fm} = 0.104$ cal/g x °C or 0.435 J/g x °C, and density $d = 8.12\ g/cm^3$

$c_{fv} = c_{fm} \times d = 3.5\ J/cm^3$

To calculate the adiabatic hot spot temperature rise ΔT, we can consider a unit of 1 cm^2 area of 2.5 microns thick foil, its volume v of $2.5 \times 10^{-4}\ cm^3$, and energy e of 0.0625 J.

$\Delta T = e/c_{fv}v = 0.01/(3.5 \times 2.5 \times 10^{-4}) = 11.4\ °C$

Calculation for NiCr Thin Film of 1/100 times foil's thickness results in an adiabatic temperature rise of 1140 °C.

STANDARDS FOR ESD TESTING OF CHIP RESISTORS

The international standard IEC 61340-3-1 describes the testing of electronic components for ESD compatibility by using the Human Body Model (HBM). Instructions for ESD testing of resistors can be found in the generic resistor specification EN 60115-1 and parameters for testing precision chip resistors - in the detail specification EN 140401-801 (see ref. 2).

This detail specification - of non-wirewound precision chip resistors (see table 2) reflects the characteristics of Thin Film chips. It defines 4 stability classes: 1, 0.5, 0.25 and 0.1 - numbers representing the allowed percentage of resistance shift for endurance (load life), for shifts due to various environmental stresses, and the permissible resistance shifts with changing ambient temperature defined by the temperature coefficient of resistance (TCR).

A test simulator conforming to the above mentioned standard produces an adjustable voltage ESD pulse by discharging a 150 pF capacitor to the device under test (DUT) with a discharge resistor of 330 Ω connected in series. These parameters differ from the ANSI/ESD 20-1999 standard which specifies a 100 pF capacitor and a 1500 Ω discharge resistor. The waveform of the ESD simulator is verified by discharging the capacitor while a 2 Ω calibration resistor replaces the DUT. The resulting pulse has therefore a time constant of:

$RC = (330 + 2) \times 150 \times 10^{-12}\ \Omega \times (s/\Omega) = 49.8 \times ns$ (compared to 150 ns, per ANSI standard).

ESD Sensitivity of Precision Chip Resistors Comparison between Foil and Thin Film Chips

The ESD exponential waveform which was calibrated with a discharge resistance of 330 + 2 Ω will have a time constant which is twice as long when the DUT is a resistor of 332 Ω and much longer with a high ohmic value DUT. Test voltages are listed in table 2. The limit of allowed change of resistance is set for all chip stability levels at 0.5 % + 0.05 Ω.

ENERGY OF ESD ABSORBED BY A RESISTOR CHIP

The ESD is simulated by charging a capacitor of C = 150 pF to a specified voltage. The stored energy $E = 0.5\ CV^2$ is discharged into two resistors connected in series: discharge resistor R_{DIS} of 330 Ω representing the resistance of a human body and R_{DUT} - of the DUT, in our case the tested chip. As a result, the following voltage V_{DUT} and energy E_{DUT} are applied to the chip:

$V_{DUT} = V \times R_{DUT}/(330 + R_{DUT})$
$E_{DUT} = E \times R_{DUT}/(330 + R_{DUT})$

Only resistors of ohmic values much higher than 330 Ω will need to absorb the full ESD energy. Low values will absorb only a small part of it. However, other factors make the low values more vulnerable:

- Low value of time constant RC results in a nearly adiabatic process and high temperature rise.
- The resistive pattern consists of a small number of pairs of lines and the voltage between adjacent end loops is higher, increasing the danger of dielectric breakdown.

CHIP RESISTOR RELATED ESD FAILURE MODES AND MECHANISMS

The ESD failures of resistors can be divided into three modes:

- Parametric: After an ESD a measurement indicates that a specified parameter, like tolerance, exceeds its prescribed limits.
- Catastrophic: The failure renders the resistor nonfunctional.
- Latent: The ESD causes a damage which does not affect resistor's performance, cannot be detected, but shortens its life.

Observed ESD failure mechanisms were:

- Stress related damage - cracking of the substrate due to thermal stresses which occur when the substrate is suddenly heated from one side by the extremely hot resistive layer.
- Dislocation or evaporation of the resistive material due to:
  - heat generated at a spot of high energy density
  - spark-over in small gaps between resistive lines - especially in patterns containing few lines and therefore a high potential difference between adjacent lines or over the kerf cut by the laser in a shunting loop.

CHOOSING PARAMETERS AND SAMPLES FOR ESD TESTING OF CHIP RESISTORS

As the Foil chips belong to a category of a much higher stability, not represented in the existing specifications, we grouped the results of our ESD tests into the following ranges of limits of resistance change:

- Less than 0.01%
- 0.01% and above but less than 0.02%
- 0.02% and above but less than 0.05%
- 0.05% and above but less than 0.1%
- 0.1% and above but less than 0.2%
- 0.2% and above but less than 0.5%
- 0.5% or higher (failure per detail specification)

For our test program we choose the RR3216M (RR1206) chip size, and two ohmic values: the lowest value of Thin Film chips - 30 Ω, which is much lower than the 330 Ω of the discharge resistor, and a second much higher value, of 1 kΩ. As other ESD test standards specify for Human Body Model (HBM) a 1500 Ω discharge resistor to simulate the ohmic resistance of a human body, the 1 kΩ DUT, in series with our 330 Ω discharge resistor, provides a waveform close to such standards.

The test voltage assigned for the 1206 size is 2 kV (see table 2), and we used this voltage as a starting point of our test, submitting the chips to gradually increased voltages up to 24 kV or up to a failure of two (or more) chips of a lot, and recording all resistance values. At each voltage level three positive and three negative pulses were applied.

In order to compare the ESD susceptibility of chips from different technologies, tests were performed on samples of 3 types:

A. Foil

B. TF1 Thin Film - nickel-chromium alloy

C. TF2 Thin Film - Tantalum nitride

Each lot contained 20 chips, bringing the total (for two values and three types) to 120 DUT.

Test equipment:

ESD simulator per IEC 61000-4-2, voltages up to 25 kV

Precision digital ohmmeter (8 digits)

Uncertainty of resistance measurements: 2 ppm + 0.001 Ω

ESD data:

One terminal connected to a horizontal grounding plate

Direct metallic contact to the second terminal

Voltages consecutively applied, KV: 2, 3, 4, 6, 8, 12, 18, 24 (highest voltage of the simulator is 25 kV).

ESD Sensitivity of Precision Chip Resistors
Comparison between Foil and Thin Film Chips

SUMMARY OF TEST RESULTS

Tables 3, 4 and 5 list the test voltages, the number of resistors which shifted by more than 0.5 % and the distribution by ranges of deviations of resistors which shifted by less than 0.5 %.

For instance, after ESD up to 24 kV, all 20 of the 30 Ω Foil chips shifted less than 0.2 %: One shifted less than 0.01 %, 3 - less than 0.02 %, 14 - less than 0.05 %, and 1 each - less than 0.1 % and 0.2 %.

- Three Thin Film lots failed the 0.5 % limit at 2 kV, the fourth at 3 kV.
- The 30 Ω Foil lot shifted less than 0.05 % at 2 kV and 3 kV, and less than 0.2 % at 24 kV.
- The 1 kΩ Foil lot shifted less then 0.01 % up to 24 kV.

TABLE 3 - 2 kV ESD DISCHARGE - COMPARISON OF DEVIATIONS, FOIL VS. THIN FILM

TYPE AND VALUE	> 0.5 %	0.2 % to 0.5 %	0.1 % to 0.2 %	0.05 % to 0.1 %	0.02 % to 0.05 %	0.01 % to 0.02 %	< 0.01 %
Foil, 30 Ω	0	0	0	0	1	6	13
TF1, 30 Ω	12	8	0	0	0	0	0
TF2. 30 Ω	0	1	1	2	8	4	4
Foil, 1000 Ω	0	0	0	0	0	0	20
TF1, 1000 Ω	20	0	0	0	0	0	0
TF2, 1000 Ω	20	0	0	0	0	0	0

TABLE 4 - 3 kV ESD DISCHARGE - COMPARISON OF DEVIATIONS, FOIL VS. THIN FILM

TYPE AND VALUE	> 0.5 %	0.2 % to 0.5 %	0.1 % to 0.2 %	0.05 % to 0.1 %	0.02 % to 0.05 %	0.01 % to 0.02 %	< 0.01 %
Foil, 30 Ω	0	0	0	0	1	8	11
TF2. 30 Ω	4	10	3	2	1	0	0
Foil, 1000 Ω	0	0	0	0	0	0	20

TABLE 5 - 24 kV ESD DISCHARGE - FOIL CHIPS ONLY

TYPE AND VALUE	> 0.5 %	0.2 % to 0.5 %	0.1 % to 0.2 %	0.05 % to 0.1 %	0.02 % to 0.05 %	0.01 % to 0.02 %	< 0.01 %
Foil, 30 Ω	0	0	1	1	14	3	1
Foil, 1000 Ω	0	0	0	0	0	0	20

CONCLUSIONS

This limited amount of testing showed a clear advantage - of two orders of magnitude - of the Foil over the Thin Film chips. Resistance shifts in Foil resistors occurred at ESD voltage levels 10 times (energy level 100 times) higher than in the Thin Film chips.

While the standard specifies for chip resistors ESD voltages of 1 kV to 3 kV according to chip's size, the foil resistors were submitted to ESD pulses of voltage up to 24 kV (as allowed by pulse simulators) without significant resistance shift: less than 0.1 % for 30 Ω and less than 0.01 % for 1000 Ω samples This voltage approaches the level obtained by walking on a synthetic carpet on a low humidity day. (We do not know the limit of energy absorbed of Foil resistors ar we do not have the equipment to reach voltages above 25 kV)

In addition to showing the superiority of Foil chips in ESD susceptibility, the test indicated non - uniformity in the behavior of Thin Film chips from different sources and different values. This may be due to the fact that their pattern design was not optimized for ESD, film deposition process was not uniform, or the substrate material was not the best. The Thin Film chips were chosen from random sources and do not necessarily represent the entire industry.

Only in recent years have ESD compatibility requirements been addressed toward resistors, and Thin Film manufacturers have started adapting their products to these requirements. Therefore it is recommended, in cases where high voltage ESD is an important requirement, to request from the chip manufacturer ESD compatibility data of their products.

ESD Sensitivity of Precision Chip Resistors
Comparison between Foil and Thin Film Chips

REFERENCES

1. Thiet The Lai: Electrostatic Discharge (ESD) Sensitivity of Thin-Film Hybrid Passive Components. IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol.12, No. 4, December 1989.
2. International Standard EN 140401-801:2002
3. F. Zandman et al.: Resistor Theory and Technology, SciTek Publishing, Inc. 2002

ACKNOWLEDGEMENT

The author would like to thank the following persons for their help in preparation of this paper

- Dr. Felix Zandman of Vishay Intertechnology for initiating and supervising this work
- Ilya Aronson, Isay Genchin, Yuval Hernik, Alex Romanow and Alex Yakir of Vishay Israel for performing the tests and assistance in preparation of the paper.
- Wolfgang Werner of Vishay Beyschlag for information about resistor standards concerning ESD in resistor standards